AMENDMENTS

In the Claims

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

1. – 11. (Canceled)

12. (Original) A method for electrically isolating a portion of a wafer comprising:

providing a first wafer;

forming a first conductor at least partially through the first wafer;

disposing first dielectric material between the first conductor and material of the first wafer; and

at least partially surrounding the first conductor and the first dielectric material with second dielectric material, the second dielectric material being spaced from the first dielectric material such that a first portion of the material of the first wafer is arranged between the first dielectric material and the second dielectric material and a second portion of the material of the first wafer is arranged outside an outer periphery of the second dielectric material.

13. (Original) The method of claim 12, wherein the first wafer has a first side and an opposing second side, and the first conductor extends through the first wafer from the first side to the second side, and further comprising:

forming a second conductor through the first wafer from the first side to the second side, the second conductor being arranged between the first dielectric material and the second dielectric material.

14. (Original) The method of claim 13, further comprising:

at least partially surrounding the second dielectric material with third dielectric material, the third dielectric material being spaced from the second dielectric material.

15. (Original) The method of claim 14, further comprising:

dicing the first wafer to form a first die assembly and a second die assembly, the first die assembly including the first conductor, the first dielectric material and a first portion of the second dielectric material, the second die assembly including the second conductor and a second portion of the second dielectric material.

16. (Original) The method of claim 13, further comprising:

providing a second wafer;

forming a first conductor at least partially through the second wafer;

disposing first dielectric material between the first conductor and material of the second wafer; and

at least partially surrounding the first conductor and the first dielectric material of the second wafer with second dielectric material, the second dielectric material of the second wafer being spaced from the first dielectric material of the second wafer such that a first portion of the material of the second wafer is arranged between the first dielectric material and the second dielectric material of the second wafer and a second portion of the

material of the second wafer is arranged outside an outer periphery of the second dielectric material of the second wafer; and

arranging the second wafer and the first wafer such that the first conductor of the first wafer and the first conductor of the second wafer electrically communicate with each other.

17. (Original) The method of claim 16, wherein the second wafer has a first side and an opposing second side, and the first conductor of the second wafer extends through the second wafer from the first side to the second side, and further comprising:

forming a second conductor through the second wafer from the first side to the second side, the second conductor of the second wafer being arranged between the first dielectric material and the second dielectric material of the second wafer.

18. (Original) The method of claim 17, wherein the first wafer includes a second conductor formed through the first wafer from the first side to the second side, the second conductor of the first wafer being arranged between the first dielectric material and the second dielectric material of the first wafer, and the first wafer and the second wafer are bonded together to form a wafer stack, and further comprising:

dicing the wafer stack to form a first die assembly and a second die assembly,

the first die assembly including the first conductor of the first wafer, the first dielectric material of the first wafer, the first conductor of the second wafer, the first dielectric material of the second wafer, a first portion of the second dielectric material of the first wafer, and a first portion of the second dielectric material of the second wafer,

the second die assembly including the second conductor of the first wafer, the second conductor of the second wafer, a second portion of the second dielectric material of the first wafer, and a second portion of the second dielectric material of the second wafer.

19. (Previously Presented) A method for electrically isolating a portion of a wafer comprising:

providing a first wafer having a first side and an opposing second side;

forming a first conductor through the first wafer from the first side to the second side;

forming a first conductor insulating layer through the first wafer, the first conductor insulating layer engaging the first conductor and being located between the first conductor and material of the first wafer, the first conductor insulating layer being formed of dielectric material; and

forming a first outer insulating layer through the first wafer from the first side to the second side and spaced from the first conductor insulating layer such that the first outer insulating layer at least partially electrically isolates the first conductor from portions of the first wafer located outside the first outer insulating layer, the first outer insulating layer being formed of dielectric material.

20. (Previously Presented) The method of claim 19, further comprising:

forming a second outer insulating layer through the first wafer from the first side to the second side and spaced from the first outer insulating layer such that the first outer insulating layer is arranged between the second outer insulating layer and the first conductor insulating layer, the second outer insulating layer being formed of dielectric material.

21. (Currently Amended) The ~~system~~ method of claim 19, further comprising:

forming a second conductor, the second conductor extending at least partially through the first wafer, the second conductor being arranged within an area at least partially bounded by the first outer insulating layer~~; and~~.

22. (Previously Presented) The method of claim 19, further comprising:

propagating a power signal via the first conductor.

23. (Previously Presented) The method of claim 19, further comprising:

propagating a data signal via the first conductor.

24. (Previously Presented) The method of claim 19, further comprising:

providing a second wafer at least partially overlying the first wafer, the second wafer having a third conductor; and

propagating a signal from the first conductor of the first wafer to the third conductor of the second wafer.

25. (Previously Presented) The method of claim 24, wherein:

the second wafer comprises:

a first conductor insulating layer formed at least partially through the second wafer, the first conductor insulating layer of the second wafer engaging the first conductor of the second wafer and being disposed between the first conductor of the second wafer and material of the second wafer, the first conductor insulating layer of the second wafer being formed of dielectric material; and

a first outer insulating layer formed at least partially through the second wafer and spaced from the first conductor insulating layer of the second wafer, the first outer insulating layer of the second wafer being formed of dielectric material.

26. (Previously Presented) A method for electrically isolating a portion of a wafer comprising:

providing a first semiconductor wafer having a substrate material; and

forming a via structure adapted to provide electrical communication through the first wafer, the via structure comprising:

first and second conductors having insulating layers to form a barrier with the substrate; and

an outer insulating layer formed about both the first and second conductors to electrically isolate the first and second conductors from the substrate material.

27. (Previously Presented) The method of claim 26, further comprising:

providing a second semiconductor wafer; and

locating the second semiconductor wafer such that the via structure provides electrical communication between the first semiconductor wafer and the second semiconductor wafer.

28. (Previously Presented) The method of claim 27, wherein:

the second semiconductor wafer comprises:

a via structure adapted to provide electrical communication through the second wafer, the via structure comprising:

first and second conductors having insulating layers to form a barrier with the substrate; and

a first outer insulating layer formed about both the first and second conductors to electrically isolate the first and second conductors from the substrate material; and

the method additionally comprises:

arranging the second semiconductor wafer in an overlying relationship with the first wafer to form wafer stack.

29. (Previously Presented) The method of claim 28, further comprising:

propagating signals between the first semiconductor wafer and the second semiconductor wafer using the via structures.

30. (Previously Presented) The method of claim 29, wherein the signals are selected from the group consisting of power signals and data signals.

31. (Previously Presented) The method of claim 26, further comprising:

propagating signals among various locations within the first wafer using the via structure of the first wafer.